WHAT IS CLAIMED IS:

1. An apparatus for determining analog error of a signal, comprising:

a first sampling switch operable to:

receive an input signal; and

sample the input signal to generate a first sampled signal;

a second sampling switch coupled to the first sampling switch by a first communication path operable to:

receive the first sampled signal from the first communication path; and

sample the first sampled signal to generate a second sampled signal;

an analog-to-digital converter coupled to the first sampling switch by a second communication path operable to:

receive the first sampled signal from the second communication path; and

produce a digital signal from the first sampled signal;

a digital memory operable to store the digital signal; and

an analog error comparison module operable to:

compare the first sampled signal to the digital signal; and

determine an analog error of the input signal based on the comparison.

2. The device of Claim 1, further comprising an analog memory operable to:

store the first sampled signal; and

provide the first sampled signal to the analog-to-digital converter after a predetermined delay.

3. The device of Claim 3, wherein:

the analog memory comprises a constant current source operable to produce a current at a constant rate; and

the predetermined delay is determined by the rate of the constant current source.

4. The device of Claim 1, wherein the first sampling switch comprises an equalization module operable to reset the first sampling switch to an initial value a predetermined time after the first sampling switch samples a value from the input signal.

5. The device of Claim 4, wherein:

the equalization module is a first equalization module; and

the second sampling switch comprises a second equalization module operable to reset the second sampling switch to an initial value for the second sampling switch a predetermined time after the second sampling switch samples a value from the first sampled signal.

6. The device of Claim 1, wherein the digital memory comprises:

a switch; and

a latch operable to latch the value of the switch.

7. The device of Claim 1, wherein:

the first sampling switch comprises at least two metal oxide semiconductor field effect transistors (MOSFETs); and

the primary carrier type of the MOSFETs is negative.

8. The device of Claim 1, wherein the input signal has a frequency of at least one gigahertz.

9. A method for determining analog error of a signal, comprising:

receiving an input signal;

sampling the input signal to generate a first sampled signal;

communicating the first sampled signal using a first communication path and a second communication path;

sampling the first sampled signal from the first communication path to generate a second sampled signal;

converting the first sampled signal from the second communication path into a digital signal;

storing the digital signal using a digital memory;

comparing the second sampled signal to the digital signal; and

determining an analog error of the input signal based on the comparison.

10. The method of Claim 9, further comprising storing the first sampled signal from the second communication path in an analog memory for a predetermined time, wherein the first sampled signal is converted to the digital signal after the first sampled signal has been stored for the predetermined time.

11. The method of Claim 10, wherein:

the analog memory comprises a constant current source operable to produce current at a constant rate; and

the predetermined time is determined by the rate of the constant current source.

12. The method of Claim 9, further comprising equalizing the first sampling switch to an initial value after the first sampling switch samples a value from the input signal.

13. The method of Claim 12, further comprising equalizing the second sampling switch to an initial value for the second sampling switch after the second sampling switch samples a value from the first sampling signal.

14. The method of Claim 9, wherein storing the digital signal comprises:

switching a switch in response to the digital signal; and

latching the value of the switch.

15. The method of Claim 9, wherein:

the step of sampling the input signal is performed by a sampling switch;

the sampling switch comprises at least two metal oxide semiconductor field effect transistors (MOSFETs); and

the primary carrier type of the MOSFETs is negative.

16. The method of Claim 9, wherein the input signal has a frequency of at least one gigahertz.

17. A circuit for determining analog error of a signal, comprising:

a first sampling switch comprising:

a first input terminal for an input signal; and

a first output terminal for a first sampled signal generated from an input signal;

a second sampling switch comprising:

a second input terminal coupled to the first output terminal of the first sampling switch by a first communication path; and

a second output terminal for a second sampled signal generated from the first sampling signal;

an analog-to-digital converter coupled to the first sampling switch by a second communication path;

a digital memory coupled to the analog-to-digital converter; and

an analog error comparison module coupled to the second output terminal of the second sampling switch and to the digital memory, the analog error comparison module comprising a third output terminal for an analog error signal generated based on a comparison of the second sampled signal with information stored in the digital memory.

18. The circuit of Claim 17, wherein the first and second sampling switches each comprise an equalization module operable to reset the respective sampling switch to an initial value.

19. The circuit of Claim 17, wherein:

the first sampling switch comprises at least two metal oxide semiconductor field effect transistors (MOSFETs); and

the primary carrier type of the MOSFETs is negative.

20. The circuit of Claim 17, wherein:

the second communication path comprises an analog memory, the analog memory comprising a constant current source producing current at a constant rate; and

the analog memory delays communication of the first sampled signal to the analog-to-digital converter by a predetermined time that is determined by the rate of the constant current source.